Please substitute the following paragraph for the paragraph at page 93, line 1. A marked up copy is provided in the attachment.

--In Table 7, impurity doses for forming the gate electrodes of the N-channel transistors T61, T62 and T63 are equally $5 \times 10^{15}/cm^2$. Phosphorus (P) is implanted as an impurity for each electrode with the implantation energy of 30 keV.--

IN THE CLAIMS

Please amend claim 18 as shown in the attachment. A clean copy is given below.

18. (Amended) The method of manufacturing a semiconductor device of claim 17, comprising:

(j) implanting nitrogen of doses n1, n2, and n3 into said control electrodes of said first, second and third transistors, respectively, where $n1 < n2 < n3$.

REMARKS

Favorable reconsideration of this application is respectfully requested.

The specification has been amended to provide correspondence between the text on pages 67 and 93 with the tables on pages 66 and 92, respectively. The objection arose from the omission of the change from "channel dope layers" to --gate electrodes-- in the preliminary amendment filed in this application. The change was made in the parent application. Withdrawal of the objection under 35 U.S.C. §132 is respectfully requested.

Claims 14-27 are present in this application. Claims 14-16 stand rejected under 35 U.S.C. §103(a) as unpatentable over U.S. 5,893,739 (Kadosh et al) in view of the book by Wolf. Claims 17 and 18 were found to be allowable if rewritten in independent form, and

claims 19-27 have been allowed. There was also an objection to the previously filed amendment under 35 U.S.C. §132 as introducing new matter into the disclosure.

First, Applicants gratefully appreciate the allowance of claims 19-27 and the finding of claims 17 and 18 to be allowable if rewritten in independent form.

Claim 14 recites forming a control electrode of a polysilicon layer of transistors on the first and second regions. This step includes the step of introducing an impurity of the same conductivity type as the source/drain layer into the polysilicon layer within the first active region at a relatively low dose, and introducing the impurity into the polysilicon layer within the second active region at a relatively high dose while introducing nitrogen into a lower portion of the polysilicon layer within the second active region. The rejection of claims 14-16 was maintained as set forth on page 3 of the previous Office Action. The Office Action takes the position that would have been obvious to include two different types of transistors in a device, specifically the transistors shown in Figures 1c-4c of Kadosh et al, where nitrogen or another barrier element is introduced into the polysilicon electrode, and a transistor such as shown in Figure 1b-4b where no nitrogen is introduced.

The Office Action points to two portions of Kadosh et al to support the argument. Column 12, lines 15-40 describe that barrier implantation is unnecessary especially when the boron implant is carefully controlled relative to a polysilicon layer thickness. Secondly, the Office Action refers to lines 10-25 of column 1, stating that different kinds of transistors are commonly formed on a single wafer. However, when these teachings (as well as the rest of the disclosure) of Kadosh et al are considered, there is clearly no suggestion of the invention recited in claims 14-16.. Both portions will be treated in turn.

The discussion in column 12, however, is directed to substitutive steps for forming a transistor and therefore, does not provide any suggestion that the two types of transistors can

be used in a single device. In fact, the Kadosh et al patent clearly teach that only one transistor is required. That is, barrier implant is a substitute for control of the the boron implant relative to the thickness of the polysilicon layer. There is no suggestion in Kadosh et al that a part of the control electrodes of a plurality of transistors is formed by barrier implantation the other electrodes are formed by controlled boron implantation.

Clearly, as Kadosh et al contain no suggestion of forming a barrier-implanted control electrode and a non-barrier implanted control electrode in the same device, the portion in column 12 of Kadosh et al does not support the rejection. In fact, it clearly teaches away from what is recited in claim 14, suggesting that the controlled non-barrier implant is an alternative to the barrier implant, without any suggestion combining the two.

Although column 1, lines 10-25 states that two types of semiconductor devices, n-type and p-type are commonly formed on a single substrate, it merely describes that impurity includes different types. There is no teaching or suggestion of the difference in impurity concentration in the gate polysilicon. There is no teaching or suggestion when introduction of nitrogen is "carefully controlled" or when barrier species is included. The outstanding Office Action does not provide any motivation or suggestion either.

In order to establish obviousness of claim 14, the Kadosh et al patent should include same suggestion for each element in claim 14. Contrary to this, the Kadosh et al patent merely provides description of the location of impurity implantation and control of impurity concentration. It is clear that there is no teaching of a relative dose of the impurity to be implanted into the polysilicon layer in the Kadosh et al.

Wolf is merely cited for forming field oxide regions, etc. and is not relied upon for the introducing of an impurity into a polysilicon layer. Claim 14 cannot be suggested by Wolf, and even in combination with Kadosh et al. In contrast to these references, the present

invention of claim 14 is directed to the formation of two types of transistors having different breakdown voltages and having the same conductivity. More particularly, the present invention has been made to solve the problems that a transistor used in a circuit system including a gate electrode receiving different voltages should be controlled in thickness of the gate oxide film and channel doping according to respective purposes, reliability of the gate oxide film may degrade during formation of the transistor.

As recited in claim 14, further, in a plurality of transistors used in a circuit system including a gate electrode receiving different voltages, an effective threshold value can be changed by establishing different impurity concentrations in the polysilicon of the gate electrode while setting the thickness of the gate oxide film to be equal, to eliminate the necessity of defining different thicknesses of the gate oxide film in accordance with difference in breakdown voltage of the transistor. The present invention of claim 14 has thereby found the solution to obtain an MOS transistor having an improved reliability of the gate oxide film and having excellent operating characteristics with simple steps of formation. Moreover, in the present invention of claim 14, when the gate electrode has a high concentration of impurity included in the polysilicon, nitrogen is introduced into the lower portion of the polysilicon. The diffusion of impurity can thereby be controlled.

For these reasons, claim 14 is clearly patentable over the applied references and is therefore in condition for allowance.

Claim 16 recites forming a control electrode which includes an impurity and nitrogen in each of the first and second transistors, that is, each of the first and second transistors has a control electrode containing an impurity in nitrogen. Claim 16 also recites the steps of masking the first type of transistor and introducing nitrogen into the control electrode of only the second type of transistor. In this case the concentration of nitrogen in the first and second

transistors would be different. The Office Action only relies upon Kadosh et al, which describes introducing nitrogen into the gate. There is no suggestion of any further implantation of nitrogen into only selected transistors. The barrier implant in Kadosh et al clearly is for each of the devices using the polysilicon layer. The barrier implant is accomplished in one step, and there is no suggestion that any further implantation of nitrogen at all should be performed let alone in a selected device while masking another device. Following the teachings of Kadosh et al one would either produce a non-barrier polysilicon control electrode or a barrier-implanted polysilicon electrode. One skilled in the art would not learn of any subsequent nitrogen implantation step or of any steps to vary the nitrogen concentration in devices from Kadosh et al.

The present Office Action refers to the discussion in the previous Office Action in rejecting claim 16. However, the previous Office Action contains no discussion regarding a method as recited in claim 16 where two devices have electrodes with different nitrogen concentrations. Accordingly, no prima facie case of obviousness of claim 16 has been made. A explanation of how each element of a claim is rendered obvious is needed to reject a claim under §103(a), and none has be made. Moreover, the lack of any disclosure or suggestion of the method of claim 16 in Kadosh et al prevents any case of obviousness to be made. Accordingly claim 16 is clearly patentably distinguishable over the Kadosh et al patent. Allowance of claim 16 is in order and is respectfully requested.

The as changes made in this amendment are only directed to matters of form, entry of the amendment is believed proper under 37 C.F.R. §1.116. Entry of this amendment is respectfully requested.

It is respectfully submitted that the present application is in condition for allowance and a favorable decision to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Gregory J. Maier
Attorney of Record
Registration No. 25,599

Carl E. Schlier
Registration No. 34,426

22850

(703) 413-3000
(703) 413-2220 (fax)
I:\atty\CES\00572534-am2.wpd

IN THE SPECIFICATION

Please amend the paragraph at page 67, line 1 as follows:

--In Table 5, impurity doses for forming the gate electrodes [channel dope layers] of the N-channel transistors T41, T42 and T43 are equally $5 \times 10^{15}/cm^2$. Phosphorus (P) is implanted as an impurity for [either layers] each electrode with the implantation energy of 30 keV.--

Please amend the paragraph at page 93, line 1 as follows:

--In Table 7, impurity doses for forming the gate electrodes [channel dope layers] of the N-channel transistors T61, T62 and T63 are equally $5 \times 10^{15}/cm^2$. Phosphorus (P) is implanted as an impurity for [either layers] each electrode with the implantation energy of 30 keV.--

IN THE CLAIMS

Please amend claim 18 as follows:

18. (Amended) The method of manufacturing a semiconductor device of claim 17, comprising:

(j) implanting nitrogen of doses n1, n2, and n3 into said control electrodes of said first, second and third [electrodes] transistors, respectively, where $n1 < n2 < n3$.